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Recommendation of Electrostatic Discharge (ESD) Control in Semiconductor Wafer Fabrication

Electrostatic Discharge is a critical yet often overlooked consideration in semiconductor wafer fabrication due to their direct impact on yield, reliability, and equipment performance. As integrated circuit geometries continue to shrink, the sensitivity of devices to electrostatic damage increases, requiring wafer fabs to implement comprehensive and proactive static control strategies. This article focuses on best practices recommended by various industry standards related to electrostatic field control. An ESD control program should be implemented throughout all stages of the manufacturing process, from photolithography to final electrical testing. Integrating electrostatic field control and charge mitigation techniques with a systematic approach focuses on equipment handler, carrier material selection (for both wafers and reticles), facility ionization and contamination control. This article aims to foster an ESD awareness and mindset to semiconductor wafer fabs. The ESD practices recommended in this article will serve as the basis for updating MIL-PRF 38535.

Why is ESD Control Crucial to Wafer Fabs?

Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA)

In semiconductor manufacturing, particularly in front-end wafer processing, Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) can cause yield loss, latent failures, and contamination. Unlike PCB assembly environments where ESD Association standards are the dominant control framework, wafer fabs deal with unique challenges due to high levels of automation, enclosed mini-environments, and complex photolithography steps involving extremely sensitive reticles.

These challenges are amplified by environmental factors such as facility humidity control, the use of insulating carrier materials, and the presence of extremely electrostatic sensitive items such as bare wafers, reticles, and advanced packaging substrates. Additionally, field-induced events are often invisible to the naked eye and may go undetected until device failure occurs during testing or after deployment, which creates tremendous reliability concerns to NASA missions.

Field-Induced Damage to Reticles

Among of the various steps involved in wafer fabrication, the reticle is by far the most susceptible component to electric field, making it particularly vulnerable to printed pattern defects. Even a low-strength, transient electric field can cause gradual and accumulative damage, creating not only catastrophic events but also latent damage risks [1].

A reticle can amplify electric fields during the photolithography process, with the fields becoming especially concentrated around the corners of the printed patterns and along the edges of the reticle. While an electric field is induced, a reticle will react to the change in the electric field condition during movement and handling. If the induced field exceeds the sensitivity of the reticle, ESD damage will occur. If the induced field occurs below the threshold voltage, field induced migration will create bridging between reticle features or meniscus, degrading reticle feature critical dimension. The extent of damage is unpredictable and depends on the structural complexity as well as the electric field orientation and strength. See Figure 1.

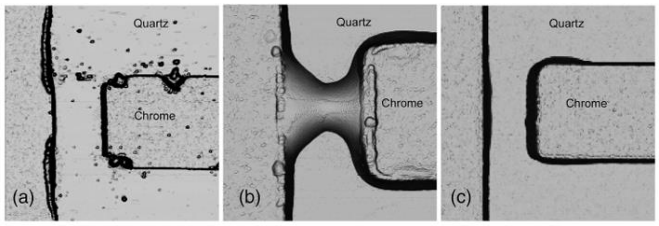

Figure 1. Reticle damage types (a) ESD damage, (b) Field-induced bridging, (c) Field-induced meniscus [2].

This has shifted the focus from the traditional ESD control approach to electric field reduction, which requires continuous monitoring of charge generation across the wafer fabrication, including equipment, facility and reticle field migration. These are discussed in the following sections.

ESD Control Implementation for Wafer Fabs

Equipment-Level ESD and ESA Control

With the advance in technology, wafers are handled in highly automatic cleanroom facilities. The facilities are constantly monitored for environmental factors, such as temperature and humidity. To achieve proper ESD/ESA protection, wafer fabs are also required to monitor equipment that is in direct contact with wafers. It is recommended that equipment should not exceed specific static charge limits. The static field limit is often tied to device technology nodes as defined by the International Roadmap for Devices and Systems (IRDS) [3], Table 1. The goal is to minimize the negative impact on productivity caused by static charges and electric fields in semiconductor manufacturing equipment [4].

Table 1 Recommended Acceptable Equipment-Induced Electrostatic Levels [3]

Year Node	*Wafers[#1] and Reticles[#2] Electrostatic Discharge, nC*	*10 pF Device[#1] Electrostatic Discharge, nC*	*10 pF Packaged Device[#1] Electrostatic Discharge, V*	*Electrostatic Field[#3], V/cm*	*V/m*	*(V/inch)*
2000 180 nm	10.0	2.5 to 10	250 to 1000	200	20,000	(500)
2004 90 nm	10.0	1.0	100	100	10,000	(250)
2010 45 nm	2.5	0.25	25	50	5,000	(125)
2017 18 nm	0.40	0.04	4.0	20	2,000	(50)
2019 17.5 nm	0.38	0.038	3.8	19	1,900	(48)
2021 17.0 nm	0.36	0.036	3.6	18.5	1,850	(46)
2024 14.0 nm	0.24	0.024	2.4	15.5	1,550	(39)
2027 11.0 nm	0.14	0.014	1.4	12	1,200	(30)
2030 8.4 nm	0.09	0.009	0.9	9	900	(23)
2033 7.7 nm	0.07	0.007	0.7	8.5	850	(21)

[#1] These table values for wafers and devices are scaled from the values for 45 nm by the square of the feature size.

[#2] These table values for reticles are scaled from the values for 45 nm by the square of the feature size. Particle values are higher.

[#3] These table values for reticles are scaled from the values for 45 nm linearly with the feature size. Particle values are higher.

To minimize static charges and electric fields, equipment owners should identify all equipment that contact wafers, reticles, or other specialized components, and select materials that generate the least charge. Ensure materials maintain electrostatic compatibility among the inter-equipment used to transfer wafers, reticles and carriers. Verify that the materials used to transport these sensitive items do not generate charges exceeding the items sensitivity. Use ANSI/ESD standard test methods to evaluate electrostatic compatibility of automated handling equipment [5], surface resistance of static dissipative planar material [6] and volume resistance measurement of static dissipative planar materials [7]. Enhance material and equipment qualification plan [8] and opt for semiconductor manufacturing equipment that meets the electrostatic compatibility recommendations in E78 [3].

Facility-Level ESD Control

The focus in this section is to expand from individual equipment to factory-wide ESD control. This provides guidance for cleanroom designers and fab operators to minimize charge accumulation on facility construction materials, personnel, and transport mechanisms. The generation of electric field causes several undesirable effects in semiconductor manufacturing environments. Wafer fab manufacturers should consider establishing allowable static field levels in the facility, proportional to the technology nodes, see table 2. Maintaining these limits can reduce particle attraction and also ESD damage. Both ESA and ESD should be taken into consideration while designing the facility for ESD control.

Table 2 Electrostatic Field Levels – Limit Particle Attraction [9]

Year Node	*d, Killer Particle Size nm*	*Electrostatic Field V/cm*	*V/m*	*(V/inch)*
2000 180 nm	90	270	27,000	(675)
2004 90 nm	45	135	13,500	(338)
2010 45 nm	22.5	67.5	6,750	(170)
2017 18 nm	9	27	2,700	(67.5)
2019 17.5 nm	8.8	26	2,600	(65)
2021 17 nm	8.5	25	2,500	(62.5)
2024 14 nm	7.	21	2,100	(53)
2027 11 nm	5.5	16	1,600	(40)
2030 8.4 nm	4.2	12.5	1,250	(31)
2033 7.7 nm	3.9	11.5	1,150	(29)

It starts with a fundamental understanding of charging levels throughout the facility. Evaluating and selecting low-charging materials for walls, floors, and furniture. Investing in high-quality instrumentation to perform measurements using industry-standard methods [9] and establishing static damage thresholds for wafers, reticles or equipment throughout the manufacturing process. Implementing proper facility monitoring for static charges, electric fields, and voltages as part of the environmental control.

Another effective measure is to utilize facility ionization systems. Air ionizers can be installed on the ceiling of the facility, in mini-environments, particularly in the product loading and unloading area at high speed, and in-line with the process equipment. It is important to emphasize that period verification of the air ionization system should be planned periodically. As the ionizer's performance decreases, unbalanced output will generate an unacceptable static charge and create ESD/ESA hazards. When electrostatic charges are neutralized by a properly balanced ionization system, electrostatic fields are reduced, consequently minimizing particle attraction. Aiding adequate air movement and particle mobility is alco crucial to minimizing particle fallout onto wafer or reticle surfaces. Once the facility's ESD control is implemented, the risk of both ESD and ESA can be significantly reduced.

Special focus on Reticle and other Electrostatic Sensitive Item Protection

There are certain components in the wafer manufacturing process considered extremely sensitive and susceptible to damage when exposed to very low electrostatic field. Reticles are a typical example of electrostatic sensitive item that requires special planning for ESD control to limit electrostatic field. See Table 3.

Table 3 Electrostatic Field Levels – Limit Induced ESD Damage on Reticles [10]

Year Node	*Electrostatic Field Limits Induced ESD Damage on Reticles, V/cm*	*V/m*	*(V/inch)*	*Electrostatic Field Limits Particle Attraction, V/cm*	*V/m*	*(V/inch)*
2000 180 nm	200	20,000	(500)	270	27,000	(675)
2004 90 nm	100	10,000	(250)	135	13,500	(338)
2010 45 nm	50	5,000	(125)	67.5	6,750	(170)
2017 18 nm	20	2,000	(50)	27	2,700	(67)
2019 17.5 nm	19	1,900	(48)	26	2,600	(65)
2021 17 nm	18.5	1,850	(46)	25	2,500	(62.5)
2024 14 nm	15.5	1,550	(39)	21	2,100	(53)
2027 11 nm	12	1,200	(30)	16	1,600	(40)
2030 8.4 nm	9	900	(23)	12.5	1,250	(31)
2033 7.7 nm	8.5	850	(21)	11.5	1,150	(29)

Protecting reticles from electrostatic discharge (ESD) and electric field-induced migration (EFM) requires tailored strategies that extend beyond traditional ESD control practices. Reticles, unlike semiconductor devices, are not electrically active and have isolated conductive features, making them uniquely vulnerable to electric field exposure. EFM occurs at field strengths far below those required to trigger ESD and is now recognized as the dominant reticle damage type [1]. It causes gradual, cumulative chrome migration on the reticle surface, degrading critical dimensions and ultimately impacting yield. While conventional ESD prevention focuses on grounding and equipotential bonding, grounding the chrome border or supporting the reticle with static-dissipative contacts may inadvertently increase internal field strength, which in turn raises the risk of EFM and ESD [10]. Instead, reticles should be supported on insulative materials to remain electrically isolated and protected from externally induced fields. It is essential to minimize disturbances in the surrounding electric field to prevent adverse effects of EFM and ESD. Ceiling-mounted air ionizers in the photolithography area of the factory

significantly reduced reticle damage. Additionally, reticle carriers should be selected carefully to provide effective shielding, protecting the reticles stored inside from exposure to electrostatic field.

As wafer feature sizes reduce and reticle pattern densities increase, EFM risk becomes more significant and cannot be mitigated by traditional ESD control alone. Therefore, the semiconductor industries must implement a reticle-specific strategy to protect against both ESD and EFM damage effectively.

Other Concerns: Contamination Risks from ESA

Electrostatic attraction, though not always resulting in electrical damage, can significantly reduce yield by attracting airborne particles onto wafer surfaces. Minimizing the generation of electric fields in a manufacturing environment is clearly necessary and the static-reduction measures currently being adopted by the industry are essential [1].

Maintaining cleanliness and minimizing electrostatic attraction (ESA) in a wafer fabrication environment is critical for safeguarding product yield and device reliability. ESA does not typically cause catastrophic damage, but it is a major source of contamination by attracting microscopic particles to wafer surfaces. These particles, especially those below than 1 µm—are significantly influenced by modest electric fields, often more so than by gravity or airflow. Charged wafers, tool surfaces, or environmental structures like plastic enclosures can create electric fields that override unidirectional airflow and drive contaminants toward critical surfaces. In addition, electric fields can penetrate containers like Front-Opening Unified Pods (FOUPs), drawing particles from inner walls onto wafer surfaces. To mitigate ESA, the control of surface charge is every wafer fab's top priority. This includes grounding conductive materials, replacing insulative items with static-dissipative alternatives, and employing targeted ionization to process essential insulators. Contaminants bonded to wafers electrostatically are incredibly difficult to remove, so prevention is far more effective than post-process cleaning. Cleanroom airflow design must also be optimized, with continuous clean airflow, avoiding field-driven particles accumulating.

Overall, contamination and ESA mitigation in wafer fabs depend on an integrated approach combining materials control, facility design, grounded equipment, and strategic ionization to ensure that clean, neutral environments are preserved throughout the facility. ESA control is equally vital as ESD prevention.

Best Practices and Implementation

There are various SEMI standards [4][9][10] and supporting studies aim to reduce wafer yield loss. In addition, ESD Association [8] also provides guidelines for facility and workstation in manufacturing facility. MIL-PRF-19500 outlines ESD program requirement for all ESD sensitive devices [11]. MIL-PRF-38535 has fundamental ESD requirements for microcircuits on the Qualified Manufacturer's List (QML) and requires ESD control at states of manufacturing process, including wafer fabrication [12]. While these existing standards offer general ESD protection or address specific aspects of manufacturing, there remains a need for a comprehensive guideline that provides an end-to-end approach to ESD control in wafer fabrication.

In summary, wafer fabs should consider the following key considerations when developing a ESD control program.

- **Minimizing electrostatic field exposure**: from equipment handling wafer to facility ESD control, wafer fabs should focus on minimizing the exposure to electrostatic field throughout the process. For EES items, such as reticles, use shielding materials for reticles carrier, minimizing movement of field induce migration, and maintain ionization both within equipment interiors and at the facility level to ensure effective charge neutralization.
- **Measuring and monitoring field levels**: utilize appropriate tools, such as field meters and particle counters, to monitor electrostatic field generation and attraction. Establish an ESD control plan proportional to the sensitivity to the area. For EES areas, such as reticle lab, enhance ESD protection by continuous monitoring of electrostatic field generation.
- **Training personnel**: despite high levels of automation in wafer fabs, personnel must fully understand the risk associated with field-induced damage, charge device model ESD damage and contamination. Training should

focus on proactive charge mitigation rather than reactive repair or cleaning.

- **Integrating ESD control across disciplines**: protective ESD measures must be integrated across multiple teams, including Quality, Manufacturing, Facilities, and Procurement to collaborate and develop practical and effective solutions for ESD protection. This cross-functional approach ensures consistent ESD protection and risk management.
- **Conducting regular audits**: perform regular ESD audits at both the equipment and facility levels to ensure ongoing compliance with the ESD control program. Audit frequency should be increased in the EES areas to strengthen protection. The audits help identify vulnerabilities, ensure corrective actions are implemented promptly and maintain a robust ESD control program.

Ultimately, the goal is to foster the mindset and behavior inside a cleanroom environment to minimize the risks of charging and contamination. An ESD control program must be practical and sustainable. This integrated approach will play a critical role in reducing yield loss and ensuring consistent wafer quality.

Case Study: A Recent ESD Audit at A Semiconductor Wafer Fab

Wafer fabs are often seen as highly automated, ultra-clean environments where state-of-the-art technology and advanced cleanrooms are deployed to eliminate human error, comparing to a traditional labor-intensive manufacturing. Given the level of advanced facility controls, it raises the question of how ESD control has been implemented in this operation?

A recent visit to a wafer facility challenged this perception. The wafer foundry is a cutting-edge class 5 cleanroom and utilizes overhead hoist systems to transport FOUPs between workstations. The facility runs fully automated, with minimal human presence. Facility environmental conditions, such as temperature, humidity, and cleanliness, are closely monitored. Operators greeted us at each workstation, presenting a clean, streamlined, and highly automated facility, exactly as we would imagine a wafer fab. What could possibly go wrong in here?

A closer review of the control plan indicated that ESD measures to prevent Charge Device Model (CDM) damage were absent. CDM occurs when a device holds a charge and then discharges upon contacting a conductive surface to equalize potential. It is the most common form of ESD damages and is especially relevant in a highly automated wafer fab. Imagine a robotic arm moving a charged wafer to a workstation at a different potential - the instant the wafer touches the surface, a discharge occurs. This can lead to latent damages, potentially compromising reliability and performance later in the product's lifecycle.
Moreover, a ESD control program must utilize proper tools to monitor charge generation and electrostatic fields. The material requirement should include the use of static dissipative materials, including wafer shipping containers and carriers. While production parameters are closely tracked, electrostatic field monitoring seems missing. There appears to be a disconnect between process control and ESD control, despite both having a significant impact on production yield and quality.

Following the first visit, there was strong interest to better understand how extremely electrostatic sensitive items, such as reticles, are handled in the facility. We visited the wafer fab again a few months later, mainly focus on the reticle lab.

The reticle lab is secured with access control, facility-wide ionization system, and protocols to protect proprietary reticle design. However, verification test revealed that the ionization system was functioning outside the required limits. In other words, the unbalanced output generated an unacceptable static charge that exceeded the ESD sensitivity threshold for the specific technology node [10].

In addition, non-ESD materials and furniture were found inside the reticle lab, and operators handle the reticles without continuous grounding monitoring. Without the proper tools to measure charge generation or electrostatic fields, the effectiveness of ESD control in such extremely electrostatic sensitive environment is uncertain. Furthermore, scanning electron microscope (SEM) used for inspection mainly focuses on visual and catastrophic defects. The awareness and ability to detect ESD or EFM associated damages have not yet been fully established.

In summary, the risk of a wafer passing electrical tests while latent failures remain undetected is considerable and could potentially lead to reliability concerns for chips developed for critical mission applications. An integrated and sustainable ESD control approach is critical for the success of NASA's missions.

Raising ESD control awareness in wafer fabs is essential, particularly monitoring and controlling electrostatic fields to prevent EFM, ESD, and ESA on sensitive items like reticles. Using industry ESD standard [8] as fundamental ESD control with tailoring to the SEMI standards emphasizing on facility, equipment and extremely electrostatic sensitive items identified in the process [13]. Wafer fabs should adopt a comprehensive approach enhancing both production yield and long-term product reliability.

Conclusions

Effective electrostatic control in wafer fabs requires an integrated, risk-based approach. SEMI standards offer a robust framework for protecting sensitive items like wafers and reticles, while ESDA standards provide complementary facility-level ESD guidance. As technology advances, fabs must refine control strategies to maintain yield, reliability, and product integrity in an increasingly sensitive environment. This article offers comprehensive and proactive approaches to wafer fabs to maintain productivity and quality while mitigating the risks of ESD damage.

The recommended practices outlined in this article will also serve as the basis for updating MIL-PRF 38535, ensuring alignment with current industry needs and best practices.

"*For wafer fabrication, an effective ESD control plan must be implemented to prevent Human Body Model (HBM) and Charged Device Model (CDM) electrostatic discharge damage. This plan should address the undesirable effects of electrostatic surface charge, which can lead to product and reticle damages, equipment malfunctions, and increased defect rates due to electrostatic discharge (ESD), electrostatic attraction (ESA)* and electric field-induced migration *(EFM). Key measures include charge mitigation plan and enhanced ESD protection in sensitive areas, specifically targeting finished wafers, reticles, and their carriers. The ESD control plan should incorporate testing methods to establish static damage thresholds for products and reticles, including measuring static charges, electrostatic fields, and voltage levels on components. Utilization of tools such as coulombmeters, electrostatic field meters, and voltmeters in accordance with SEMI standards (E78, E129 & E163) will provide necessary evaluations. These assessments to ensure effective monitoring and control of electrostatic discharge risks. Additionally, manufacturer shall perform ESD audit per S20.20 with tailoring to the wafer production to ensure compliance to ESD control plan in all ESD protected areas (EPAs)*."

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