National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the JPL/OSMS Assurance Technology Program Office (ATPO), NASA EEE Parts Assurance Group (NEPAG), and Section 514, of the Jet Propulsion Laboratory.

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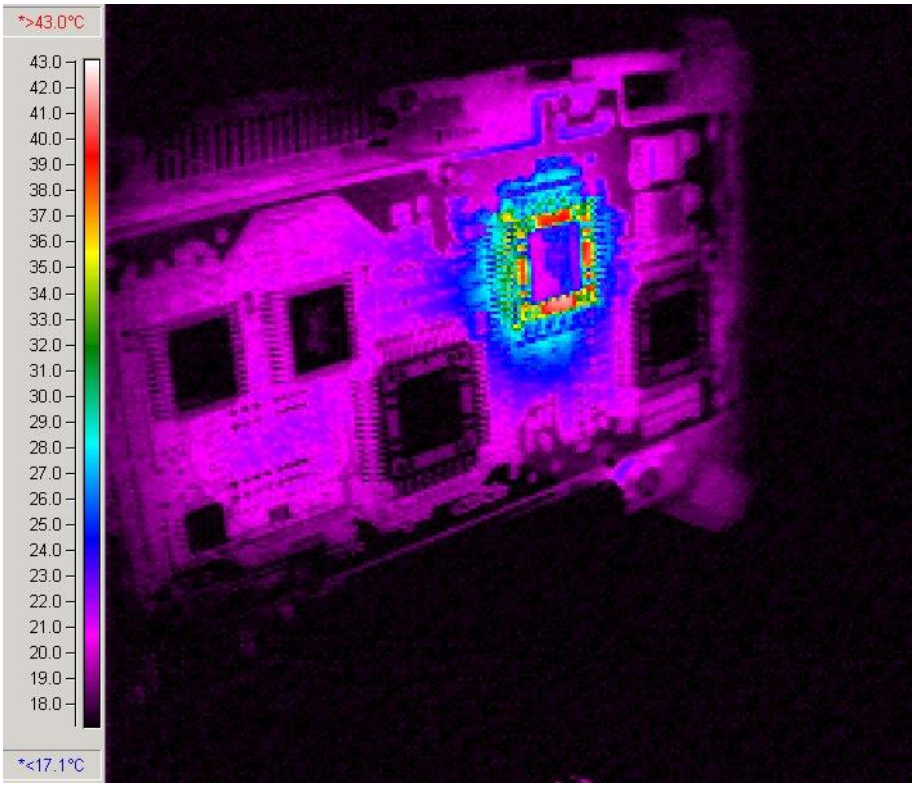

Short-wave infrared image showing an application-specific integrated circuit (ASIC) that had a bus contention problem at a low temperature causing it to malfunction. An infrared camera placed inside the oven precisely located the device failure point when the downward-cycling oven reached 16°C. The device was later replaced, and the spacecraft hardware worked throughout the mission.

Capturing a Failure of an ASIC in-situ Using Infrared Radiometry and Image Processing Software

Non-destructive-evaluation (NDE) methods for detecting electronic failures and anomalies encompass a host of novel instrumentation methods and techniques. Infrared (IR) radiometry is a non-contact method used for locating hot spots and surface temperature differences of materials that emit IR in the short and medium wave bands of 3.5–5.0 microns or 8–12 microns. The image above was produced using an IR camera in the short wave band together with software adjusted to capture temperature changes in flight hardware during the cooling cycle of a burn-in test. This method of identifying the anomalous behavior of an ASIC was done with only one day for set-up and testing. In contrast, other probing and testing methods may have required two weeks to locate the failed device.

This note is excerpted from a more detailed article of the same name in *InfraMation 2003*, Infrared Training Center, Billerica, MA, http://www.infraredtraining.com/.

A link to access the article is

http://trs-new.jpl.nasa.gov/dspace/bitstream/2014/39015/1/03-2512.pdf

Personnel from JPL performed the IR radiometry for the Galaxy Evolution Explorer (GALEX) project, which was assembling an ultraviolet space telescope in 2002.

Infrared radiometry was a relatively new technique for microelectronic parts at the time. Since then, the technique has matured and is now incorporated into the radiometers themselves. Furthermore, this method of isolating hotspots by image subtraction is increasingly being used in medicine, architectural building inspection, and aerospace.

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Potential Threat to Printed Wiring Boards

Is there a potential risk of manufacturing printed circuits with surreptitiously introduced extra circuitry that could allow unauthorized access?

Printed Wiring Boards (PWB, also referred to as printed circuit boards, PCB) have become very complicated. In the last 10 years, board area has remained relatively constant while the number of leads per square inch has tripled. In addition, the average number of components has quadrupled in 15 years while the average leads-per-part has decreased by a factor of 4–5x. This reflects the increasing use of a few very high pin-count parts. The number of pins in a design has tripled, and the number of pin-to-pin connections has doubled.

A high percentage of PWBs is now being manufactured with multilayers and high-density circuitry embedded within several board layers to support advanced electronic component technology.

(For more information on PWB complexity, see http://www.techdesignforums.com/practice/technique/overcoming-increasing-pcb-complexity-with-automation.)

Because many PWBs are so highly complex, a few altered circuits could easily go unnoticed.

Circuit design may potentially be altered in such a manner that it can intentionally provide a possible connection to expose a “backdoor” or connection into an electronic component leaving this component at risk of being accessed remotely at a later time with the intent of exercising a malicious act. Such remote component manipulation leaves the system liable to theft of data, implanting of false data, and possibly a major system failure either through deliberate sabotage by an intruder or the introduction of problem instructions. Such damage could result in costly failures, conceivably something as great as mission failure with costs in the billions of dollars.

One potential method for achieving such access is by altering the Gerber data, which is the data package describing the PWB images, copper layers, and even electrical test information. Such data is typically supplied by the customer to the manufacturing facility. Essentially, the Gerber data file contains the artwork depicting the circuit design that is printed and subsequently sent through the manufacturing processes to produce the PWB. Gerber data may be modified in some way to include additional circuitry that can be used for access into very expensive and delicate electronic components such as a Field Programmable Gate Array (FPGA) on the PWB.

In such a situation, the offender may extract configuration data, access keys and other information from the exposed component, including unencrypted configuration bitstream, and permanently damage the device.

Should a modified PWB design be detected, the resulting PWB assembly can be considered a counterfeit board by definition of the Defense Federal Acquisition Regulation Supplement (DFARS case 2012 D055), which states, “…an unauthorized reproduction, substitution, or alteration that has been knowingly mismarked, misidentified, or otherwise misrepresented.” Since its integrity has been compromised, the board no longer holds the intended design and may not meet the requirements.

A possible risk mitigation approach for detecting altered Gerber data is to implement verification and/or validation to confirm that all circuit design data for each board layer is legitimate prior to printing the artwork and before starting PWB manufacturing. Careful examination, and then seeking concurrence/approval by the customer on the final artwork, will heighten assurance for a conforming printed circuit product.

Such verification could be incorporated into military specification PWB audits (also by and often involving the space community working with DLA Land and Maritime) to ensure the integrity of all Gerber data being supplied and transferred to the manufacturer’s system, ensuring that the data remains unchanged before the manufacturing processes begin.

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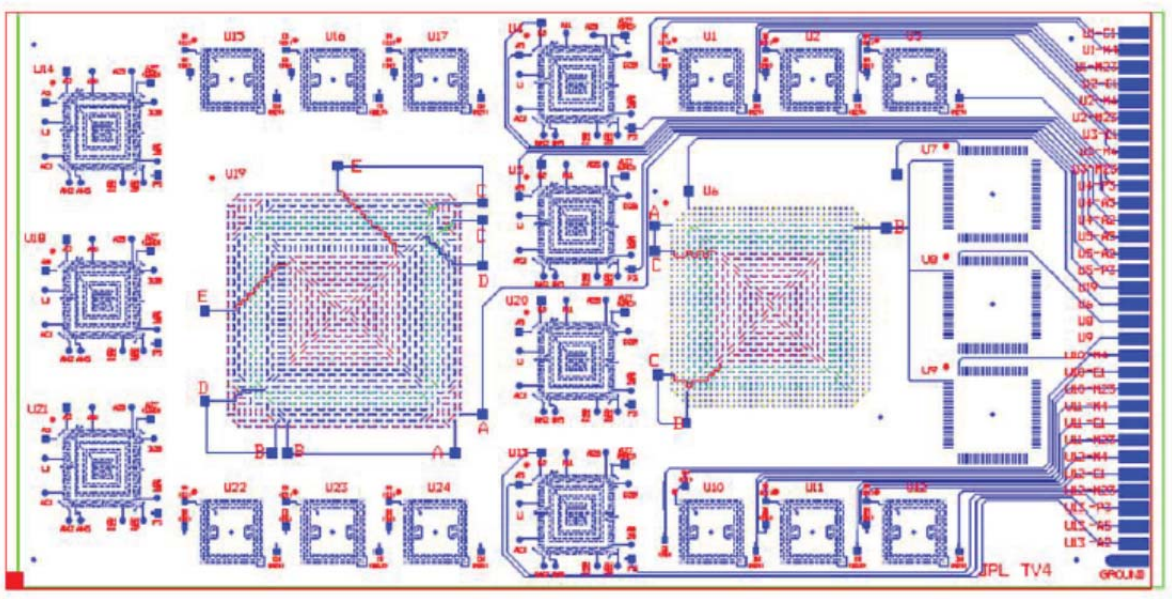
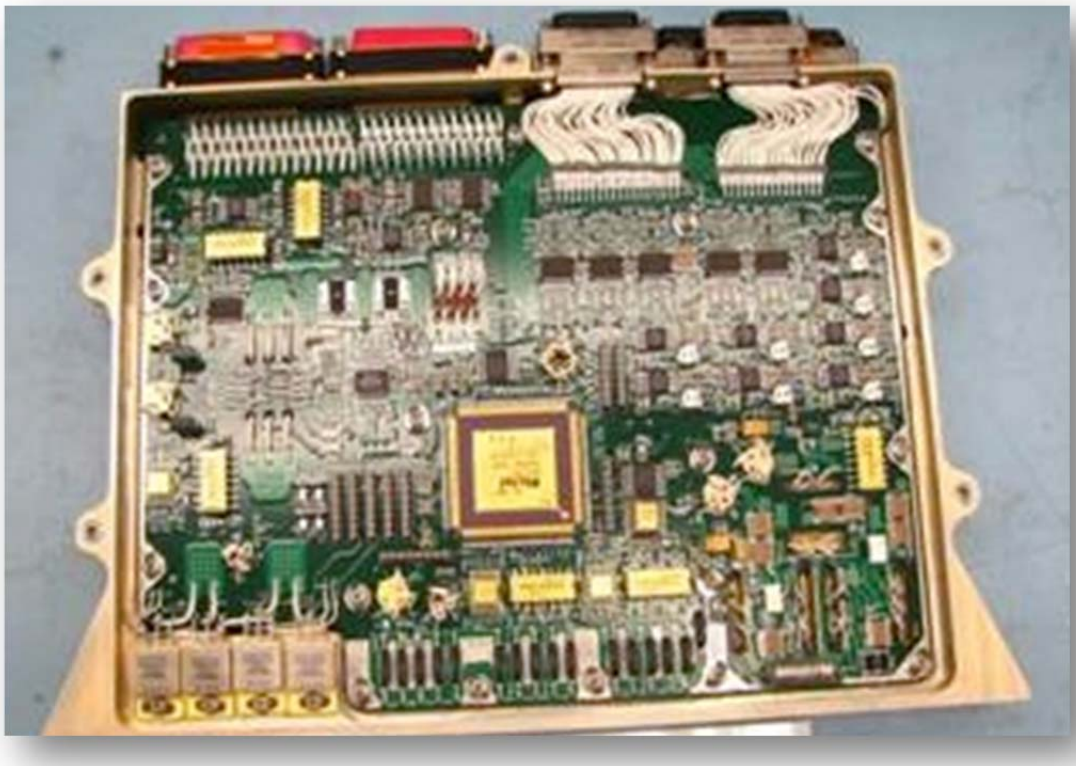


PWB Diagram showing typical complexity of one layer. This PWB has 0.93 mm thickness required to accommodate microvias for lower I/O finer pitch ball grid array (100–400 input/outputs (I/Os) and 0.3–0.4 mm pitches) (from R. Ghaffarrian, Reliability of CGA/LGA/HDI Package Board/Assembly, JPL Publication 12-3, Rev. A, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, Feb. 2012, http://trs-new.jpl.nasa.gov/dspace/bitstream/2014/41966/3/JPL%20Pub%2012-3%20Rev%20A.pdf).



PWB for battery control of the Mars Science Laboratory rover is more complex but comparable to a PWB for an electric automobile. This board has been populated with a large number of interconnections and an FPGA (from Mars Science Laboratory project, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California).

NASA Parts Specialists Recent Support for DLA Land and Maritime Audits:

Audits performed at

- Ardentec, Hsinchu, Taiwan
- AVX Tantalum Corp., Biddeford, ME
- Hamby Corporation, Valencia, CA
- L-3 Communications, Mason, OH
- Micropac Industries, Inc., Garland, TX
- UMC (MSC/Actel, Atmel), Hsinchu and Tainan, Taiwan
- International Rectifier, Leominster, MA
- Semicoa Corporation, Costa Mesa, CA
- Corwil Technology Corporation, San Jose, CA

Upcoming Meetings

- EEE Parts for Small Missions, Goddard Space Flight Center, Greenbelt, MD, Sept. 10–11, 2014
- JC-13 / G-12 / G-11 Committee Meetings; Columbus Renaissance, Columbus, OH, Sept. 15–18, 2014
- 27th Microelectronics Workshop (MEWS27), Tsukuba, Japan, Oct. 23–24, 2014

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