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Class Y, a new Class of Space Microcircuits

Advances in packaging and device technology are happening rapidly. How do we enable space flight projects to benefit from the newly developed devices?

On December 20, 2013, the Defense Logistics Agency (DLA) released Revision K of microcircuit specification, MIL-PRF-38535. This is significant because it introduces Class Y, a new category of ceramic-based non-hermetic microcircuits for space (including Xilinx Corporation Virtex-4 and Virtex-5 field programmable gate arrays [FPGAs] and similar devices from other suppliers).

Development of Class Y was a NASA-led initiative for the world-wide space community to infuse new technology into military/space standards.

Creation of this new class of microcircuits required considerable effort (see Figure 1). It was coordinated with manufacturers, government agencies, prime contractors, and other interested entities (e.g., academia). Also, we needed to ensure that all aspects of packaging configuration were adequately covered by the military documents, such as MIL-PRF-38535 and MIL-STD-883. These packaging aspects included flip-chips, underfills, adhesives, column attaches, and others

New test methods were created, and the existing standards were updated. Some of the work is continuing. The left column of Figure 1 shows the path to standard space (QMLY) flight parts procurement. For further information, contact:

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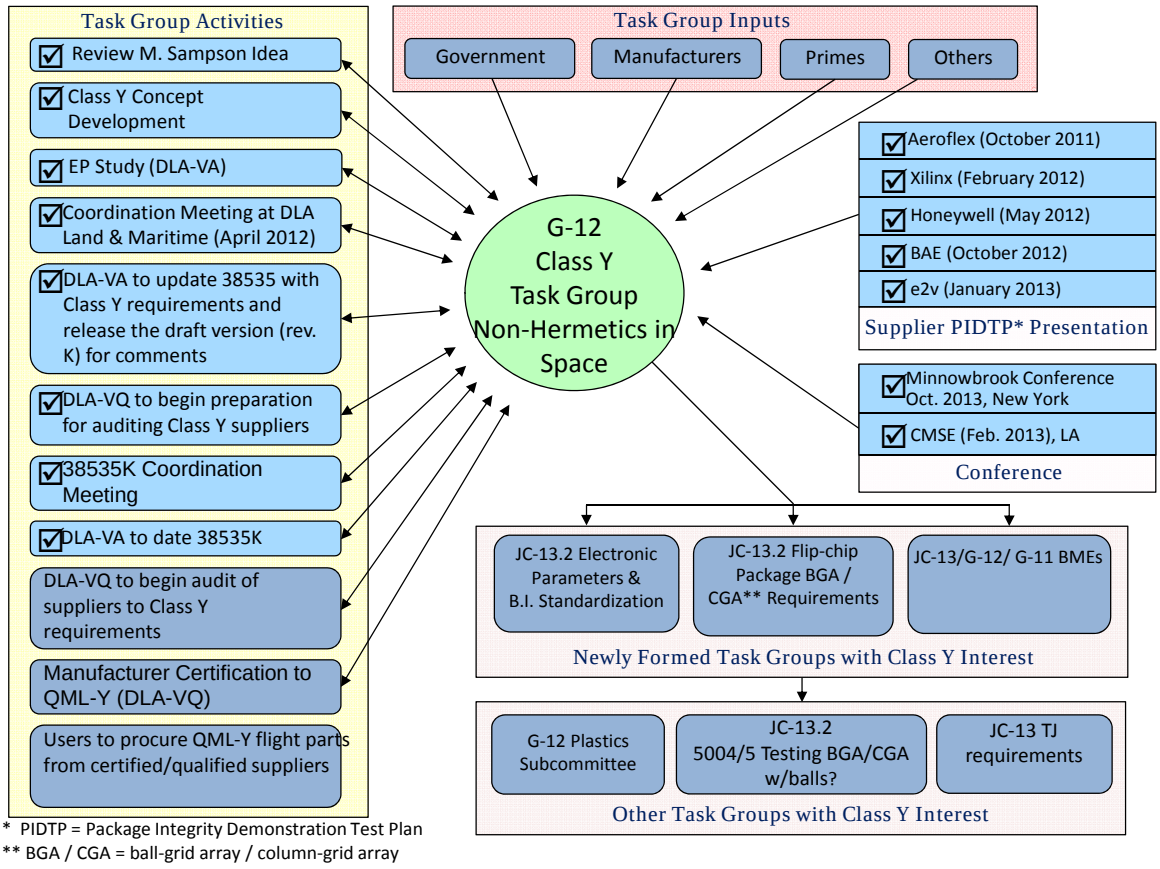

Figure 1. Infusion of New Technology into the QML System G12 Class Y Effort at a Glance

Inspection and Testing of BME Capacitors Mounted on High Input/Output Column-Grid Arrays and on Printed Circuit Boards

Base metal electrode (BME) capacitors were developed for meeting microelectronic industry needs to reduce cost, increase capacitance, and reduce size. Manufacturers of newer products are increasingly using BMEs.

However, BMEs present quality concerns because they are a new technology and because they attain greater capacity via a significantly greater number of thinner capacitance layers. Thus, greater use of BMEs is contingent on developing testing methods tailored to them.

The Jet Propulsion Laboratory (JPL) conducted an exercise in inspection and testing of BME solder joints in column grid array (CGA) packages as delivered, after thermal-shock cycling, and after mounting assemblies on a printed circuit board (PCB) and then thermal cycling.

Figure 2 shows a generic schematic construction of a non-hermetic CGA package with 1752 pure-solder-alloy columns, a representative of the previous generation of CGA surface-mounted packages that were inspected and tested. The lower part of the figure shows two top-down images of a typical CGA package. The lower left is an optical photograph, and the right is an X-ray image. These images clearly show a number of the BME capacitors surrounding the heat sink on the die. The new generation of the package (CN) will limit inspection of the BME capacitors due to extension of the heat sink over the substrate.

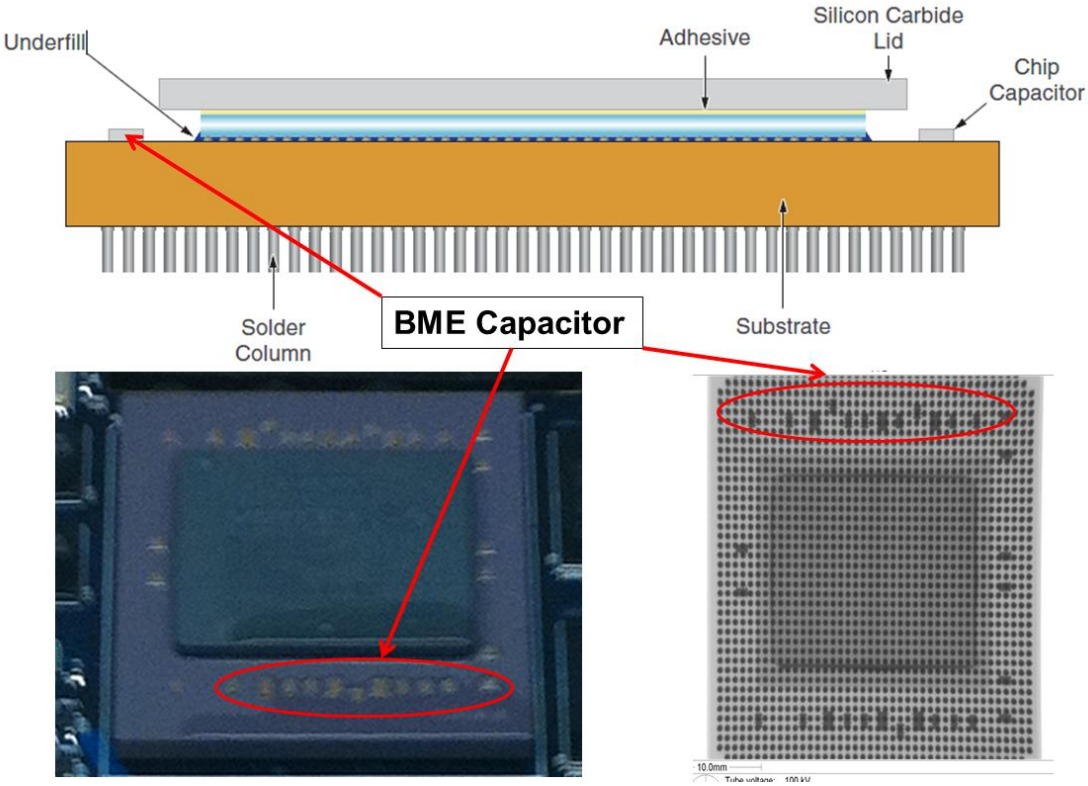

Figure 2. Construction of generic CGA 1752 I/O package (top) and photographs of a typical CGA package with optical (left) and X-ray (right) showing the exposed BME capacitors.

Five daisy-chain (nonfunctional or mechanical) input/output (I/O) CGA packages with BME capacitors were procured for developing procedures for inspection and testing. These packages came soldered onto the substrate of ceramic column grid array (CGA) packages.

No apparent failures were observed in the five BME capacitors either externally at the solder joints or internally within the cross-sectioned capacitors after the as-received CGAs were subjected to thermal-shock cycling and the as-assembled CGAs were subjected to thermal cycling. Even though SEM inspection of the BME solder joints and of cross sections showed degradation due to thermal exposures, no severe microcracking or separation was apparent.

Qualification procedures such as these, combined with reliability test data, will help NASA project teams gain confidence in the use of higher density electronics packages such as the CGA packages examined in this inspection and testing exercise.

The inspection and testing are detailed in *Reliability of CGA/LGA/HDI Package Board/Assembly*, JPL Publications 12-3, Revision A. That publication is also available on the NEPP website at https://nepp.nasa.gov/. For further information, contact:

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GIDEP Alerts/Advisories

Contact your GIDEP Representative for a copy of:

Suspect Counterfeit	AAN-U-13-400 Suspect Counterfeit, Microcircuit, Linear; AAN-U-13-400A Suspect Counterfeit, Microcircuit, Linear; BDR-A-13-02 Suspect Counterfeit, Microcircuit, Digital, Quiet Series Octal Bidirectional Transceiver; BDR-A-13-03 Suspect Counterfeit, Microcircuit, Digital, CMOS Programmable Interval Timer; BDR-A-13-04 Suspect Counterfeit, Microcircuit, Digital-Linear, 12-Bit Analog Converter; BDR-A-13-05 Suspect Counterfeit, Microcircuit, 1-Micron CMOS 12-Macrocell PLD; BDR-A-13-06 Suspect Counterfeit, Microcircuit, Linear, CMOS Analog Switch; BDR-A-13-07 Suspect Counterfeit, Microcircuit, Linear, Monolithic CMOS Analog Multiplexer; BDR-A-13-08 Suspect Counterfeit, Microcircuit, Linear, JFET Input Operational Amplifier; BDR-A-13-09 Suspect Counterfeit, Microcircuit, Linear, JFET Input Operational Amplifier; BVZ-A-13-01 Suspect Counterfeit, Microcircuit, 5V Byte Alterable EEPROM; CEW-P-13-01 Suspect Counterfeit, Integrated Circuits, CPLD; CLS-P-14-01 Suspect Counterfeit, Microcircuit, +5V CMOS, RS-232 100KBPS, Transceiver with 2 Drivers/Receivers; EB9-A-12-01A Suspect Counterfeit, Microcircuit, NOVRAM, 2K X 8 Bit; EF2-P-13-01 Suspect Counterfeit, Semiconductor Device, Thyristore; C9Y-A-13-01 Suspect Counterfeit, Integrated Circuit; C9Y-A-14-01 Suspect Counterfeit, Microcircuit, Integrated Circuit; CLS-P-14-01 Suspect Counterfeit, Microcircuit, +5V CMOS, RS-232 100KBPS, Transceiver with 2 Drivers/Receivers; E1C-A-13-01 Suspect Counterfeit, Microcircuit, NOVRAM, 2k X 8 Bit; GG5-A-14-01 Suspect Counterfeit, Microcircuit, N-Channel MOSFET; PY4-A-13-01 Suspect Counterfeit, Microcircuit, Memory; VN4-A-14-01 Suspect Counterfeit, Microcircuit, Linear, Operational Amplifier

NASA Parts Specialists Recent Support for DLA Land and Maritime Audits:

Audits performed at ADI, Limerick, Ireland; Cypress Semiconductor, San Jose, CA; Crane Electronics, Redmond, WA; TE Connectivity (formerly Deutsch ECD), Oceanside, CA; Teledyne Microwave Solutions, Mountain View, CA; Teledyne Microelectronics Technology, Lewisburg, TN; Semicoa Corp., Costa Mesa, CA; Murrieta Circuits, Anaheim, CA.

Upcoming Meetings

- JEDEC JC-13, Las Vegas, NV, Jan. 13–16, 2014
- JEDEC JC-13, Minneapolis, MN, May 19–22, 2014

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http://atpo.jpl.nasa.gov/nepag/index.html

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